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EXAMINER
JOSEPH, JAISON

ART UNIT	PAPER NUMBER
2611	

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11/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/642,259	LEE ET AL.	
	Examiner	Art Unit	
	Jaison Joseph	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-33 and 40* is/are allowed.

6)☒ Claim(s) *1-6,11-14,22,34,35 and 38-42* is/are rejected.

7)☒ Claim(s) *7-10,15-21,36,37,43 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 08/30/2007 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argue, Neither Momtaz or Chung teaches or suggests ... determinable from Momtaz or any other reference of record". However Examiner respectfully disagrees. Momtaz does teach the limitations of "phase detection circuitry configured to generate feedback indicative of the amount of jitter" as recited in claim 1 (see figure 1, phase detector 11). According to Newton's Telecom Dictionary, the definition of jitter is "phase shift of digital pulses over a transmission medium". This is phase difference of two pulses i.e. phase difference between received and sampling pulses. Momtaz clearly teach the cited limitations of "phase detection circuitry configured to generate feedback indicative of the amount of jitter" in figure 1 (see figure 1, component 11, the output of the phase detector represent the phase difference between the received data and the data sampling clock). Therefore Momtaz in view of Chang teach all cited limitations. Thus Examiner maintains the rejection of claims 1 - 6, 11 -14, 22 - 25, and 38 - 42. Furthermore, Applicant is reminded that the examiner is entitled to give broadest reasonable interpretation to the language of the claims.

Regarding claim 34 and 35, Applicant argues, "Claim 34 recites a jitter estimating circuit ... is patentable over Saitoh." However Examiner respectfully disagrees. Saitoh et al each a jitter estimating circuit for use in an clock and data recovery device configured to generate samples of data having jitter using a data sampling clock, where the clock

and data recovery device is configured to generate the data sampling clock by applying variable delay to a first clock in response to feedback indicative of phase error between the data sampling clock and the data (see figure 3), said circuit including: counter circuitry configured to generate a sequence of counts in response to the feedback (see figure 3, component 42), wherein each of the counts is indicative of the number of times that the clock and data recovery device changes the phase of the first clock during a predetermined number of valid transitions of the data; and decision logic (see figure 3, component 43), coupled to the counter circuitry and configured to generate code words in response to the counts, wherein the counts have values in a range of count values, the range is partitioned into segments, and each of the code words is generated in response to one of the counts and indicates one of the segments to which said one of the counts belongs (see column 4, lines 15 – 47). Further component 42 counts up or down according to the U/D signal from component 41. U/D signal is indicative of the phase changes the phase of the first clock during a predetermined number of valid transitions of the data (see figure 8 and 9). Component 42 counts the changes (either count up or count down) based on the enable signal from component 41 (See figure 3). Thus Saitoh teach all cited limitations. Therefore Examiner maintains the rejection of claim 34 and 35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 6, 11-14, 22 – 25, and 38 – 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz (US Patent 5,945,855) in view of Chang (USPAP 2002/0027457).

Regarding claim 1, Momtaz teaches A clock and data recovery device for generating data samples in response to data having jitter, said device including: sampling circuitry coupled and configured to receive the data and to generate the data samples (see figure 1, data detector); clock generation circuitry configured to generate the data sampling clock in response to at least one control signal and to assert the data sampling clock to the sampling circuitry (see figure 1, VCO 14), wherein the phase of said data sampling clock is determined by the control signal (the phase of the clock signal is controlled by the phase detecting circuit); phase detection circuitry configured to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data (see figure 1, phase detector 11); and clock control circuitry, coupled and configured to generate the control signal in response to the feedback and to assert the control signal to the clock generation circuitry (see the charge pump and loop filter), wherein the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕav is nonzero (see the up and down signals), where Iav is an average of instantaneous values of the phase error between the data sampling clock and the data over the time

interval(see the up and down signals). Momtaz does not expressly teach the sampling circuitry employ over 2x over sampling using plurality of clock signals. However in analogous art Chang et al teach a over sampling circuitry, over samples data using two clocks to generate a 2x over sampled data signals (see paragraph 13). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to replace Momtaz's over sampling circuitry with Chang's over sampling circuitry. The motivation or suggestion to do so is to have a simple dounle data rate sampler.

Regarding claim 2, which inherits the limitations of claim 1, Momtaz further teaches wherein the clock generation circuitry is a voltage controlled oscillator, the clock control circuitry includes a charge pump circuit, and the charge pump circuit is configured to generate a charge pump current in response to the feedback and to generate the control signal in response to the charge pump current (see figure 1, components 11, 12, 13, 14), wherein the charge pump current has an average current value, Iavg, that is at least substantially independent of the amount of the jitter over said each time interval over which ϕav is nonzero, where Iavg is an average of instantaneous values of the charge pump current over the time interval (see up and down signals).

Regarding claim 3, which inherits the limitations of claim 2, Momtaz further teaches wherein the charge pump circuit is configured to generate the charge pump current such that said charge pump current has an absolute value that is proportional to the amount of the jitter (see column 3, lines 59 –63).

Regarding claim 4, which inherits the limitations of claim 2, Momtaz further teaches wherein the average current value, Iav is independent of the amount of the jitter over said each time interval over which ϕav is nonzero (see column 3, lines 59 –63).

Regarding claim 5, which inherits the limitations of claim 2, Momtaz further teaches wherein the feedback is indicative of a sequence of control bit pairs, a first bit in each of the pairs is indicative of whether the phase error between the data sampling clock and the data is positive, a second bit in each of the pairs is indicative of whether said phase error is negative (see figure 1, up and down signals); and the charge pump circuit includes: a first node coupled to receive a first signal indicative of the first bit of each of the control bit pairs (output up signal); a second node coupled to receive a second signal indicative of the second bit of each of the control bit pairs (output down signal); delay circuitry coupled to receive the first signal and the second signal and configured to assert in response thereto a first delayed signal indicative of the first bit of each of the control bit pairs and a second delayed signal indicative of the second bit of each of the control bit pairs (see figure 4, delay circuits); a third node (see figure 4, output of charge pump circuit); and additional circuitry, coupled to the first node, the second node, the delay circuitry, and the third node, and configured to source a positive current to the third node when one of the control bit pairs indicates positive phase error but does not indicate negative phase error between the data sampling clock and the data, and to sink a current from the third node when one of the control bit pairs indicates negative phase error but does not indicate positive phase error between the data

sampling clock and the data (see figure 4, charge pump circuit and column 6, lines 50 – column 7, lines 11).

Regarding claim 6, which inherits the limitations of claim 5, Momtaz further teaches wherein the second signal is indicative of the complement of the second bit of each of the charge pump control bit pairs, the delay circuitry includes a first inverter whose input is the first node and a second inverter whose input is the second node, the first inverter has an output coupled to assert the first delayed signal to the additional circuitry, and the second inverter has an output coupled to assert the second delayed signal to the additional circuitry (see figure 4, charge pump circuit and column 6, lines 50 – column 7, lines 11).

Regarding claim 11, which inherits ht limitations of claim 1, the combination of Momtaz and Chang does not expressly teach the data sampling frequency equal to f/N. However at the time the invention was made it would have been to a person of ordinary skilled in the art to realize the sampling frequency is f/N. since applicant have not disclosed having the frequency f/N provides an advantage, is used for a particular purpose or solves a stated problem. Therefore, it would be obvious to one of ordinary skilled in the art to modify the combination of Momtaz and Chen to obtain the invention as specified in claim 11.

Regarding claim 12, the claimed device including the features correspond to subject matter mentioned in the rejection claim 1, is applicable hereto.

Regarding claim 13, which inherits the limitations of claim 12, the claimed device including the features correspond to subject matter mentioned in the rejection claim 2, is applicable hereto.

Regarding claim 13, which inherits the limitations of claim 12, the claimed device including the features correspond to subject matter mentioned in the rejection claim 3, is applicable hereto.

Regarding claim 22, which inherits the limitations of claim 12, Momtaz further teaches wherein the clock generation circuitry is a voltage controlled oscillator, and the clock control circuitry is configured to assert a control voltage, determined by the charge pump current, to the clock generation circuitry (see figure 1).

Regarding claim 23, which inherits the limitations of claim 12, the claimed device including the features correspond to subject matter mentioned in the rejection claim 5, is applicable hereto.

Regarding claim 24, which inherits the limitations of claim 23, the claimed device including the features correspond to subject matter mentioned in the rejection claim 6, is applicable hereto.

Regarding claim 25, which inherits the limitations of claim 12, the claimed device including the features correspond to subject matter mentioned in the rejection claim 11, is applicable hereto.

Regarding claim 38, the claimed device including the features correspond to subject matter mentioned in the rejection claim 1, is applicable hereto.

Regarding claim 39, the claimed device including the features correspond to subject matter mentioned in the rejection claim 1, is applicable hereto.

Regarding claim 41, the claimed device including the features correspond to subject matter mentioned in the rejection claim 1, is applicable hereto.

Regarding claim 42, which inherits the limitations of claim 41, the claimed device including the features correspond to subject matter mentioned in the rejection claim 3, is applicable hereto.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 34 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitoh et al (US Patent 5,604,775).

Regarding claim 34 and 35, Saitoh et al each a jitter estimating circuit for use in an clock and data recovery device configured to generate samples of data having jitter using a data sampling clock, where the clock and data recovery device is configured to generate the data sampling clock by applying variable delay to a first clock in response to feedback indicative of phase error between the data sampling clock and the data (see figure 3), said circuit including: counter circuitry configured to generate a sequence of

counts in response to the feedback (see figure 3, component 42), wherein each of the counts is indicative of the number of times that the clock and data recovery device changes the phase of the first clock during a predetermined number of valid transitions of the data; and decision logic (see figure 3, component 43), coupled to the counter circuitry and configured to generate code words in response to the counts, wherein the counts have values in a range of count values, the range is partitioned into segments, and each of the code words is generated in response to one of the counts and indicates one of the segments to which said one of the counts belongs (see column 4, lines 15 – 47).

Allowable Subject Matter

Claims 26 – 33 and 40 are allowable over prior art of record.

Claims 7 – 10, 15 – 22, 36 – 37, 43 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jaison Joseph
11/09/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER